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Ferroelectric properties of $SrBi_2Ta_2O_9$ thin films on Si (100) with a $LaZrO_x$ buffer layer

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Abstract To obtain a metal–ferroelectric–insulator–semiconductor (MFIS) structure, we fabricated ferroelectric $SrBi_2Ta_2O_9$ (SBT) film on a p-type Si (100) wafer with a $LaZrO_x$ (LZO) buffer layer by means of a sol–gel technique. The sol–gel deposited LZO film according to the different annealing temperatures had a good surface morphology even though the crystalline phase was not an amorphous phase. In particular, the root-mean-squared (RMS) surface roughness of the 750-°C-annealed LZO film was about 0.365 nm and its leakage current density was about 8.2×10^{-7} A/cm^2 at 10 V. A Au/SBT/LZO/Si structure with different SBT film was fabricated. The *C–V* characteristics of the Au/SBT/LZO/Si structure showed a clockwise hysteresis loop. The memory window width increased as the SBT film thickness increased. The 600-nm-thick SBT film was crystallized in a polycrystalline phase with a highly preferred (115) orientation. The memory window width of the 600-nm-thick SBT film was about 1.94 V at the bias sweep voltage ±9 V and the leakage current density was about 6.48×10^{-8} A/cm^2 at 10 V.

Keywords MFIS · $SrBi_2Ta_2O_9$ · $LaZrO_x$ · Sol–gel

1 Introduction

Many studies have been extensively investigated for ferroelectric random access memory (FeRAM) as promising for the next generation non-volatile memories. Metal–ferroelectric–semiconductor field-effect transistors (MFSFETs) with a single transistor (1-T) memory cell have promising advantages of high density integration, a non-destructive read-out operation, low power-consumption, and high-speed operation [1, 2]. Despite their superior advantages, however, these MFSFETs have not yet been commercialized. MFSFETs, where ferroelectric thin film is directly deposited on a silicon substrate, have some problems. These problems are, for example, interdiffusion of constituent elements, formation of an amorphous SiO_2 layer with a low-k dielectric constant at the interface of the ferroelectric film and Si substrate and crystalline quality degradation [3]. To solve these problems, we propose a metal–ferroelectric–insulator–semiconductor (MFIS) structure with a good insulator that works as buffer between the ferroelectric layer and Si substrate [4]. Most of insulating buffer layers used in a MFIS structure have a high dielectric constant in the range of 10–50, low leakage current, and good interface characteristics. As representative insulating buffer layers, there are ZrO_2, HfO_2, $HfAlO_x$, $LaAlO_3$, and so on [5–8].

Recently, $LaZrO_x$ (LZO) thin film applied as buffer layer for the superconductor $YB_{a2}Cu_3O_{7-\delta}$ (YBCO) has been reported to have a high crystallization temperature and relatively high dielectric constant of ≈20. Also, both lanthanum and zirconium atoms, the constituents of $LaZrO_x$ thin film, have been considered as being thermally stable in contact with Si [9]. In particular, it has been reported that LZO thin film has a cubic pyrochlore structure with a lattice parameter which leads to a mismatch of 0.68% with Si ($2a_{Si}$= 10.86 Å) [10]. Therefore, we think that the LZO thin film acts as a suitable insulating buffer layer in a MFIS structure.

Ferroelectric thin films such as $SrBi_2Ta_2O_9$, $Pb(Zr,Ti)O_3$, $Bi_4Ti_3O_{12}$, $(Bi,La)_4Ti_3O_{12}$, or $Pb_5Ge_3O_{11}$ have been exten-

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sively investigated for non-volatile FeRAM devices [11–15]. As a ferroelectric layer, we chose the $SrBi_2Ta_2O_9$ (SBT) film for a MFIS structure. The SBT film is one of the most promising candidates for a 1-T type FeRAM because of its high fatigue endurance, good retention, and low leakage current [16].

In our study, we fabricated the LZO/Si and the SBT/LZO/Si structures using a sol–gel method. Then, we investigated their physical and electrical properties. From these measurements, we evaluated the feasibility of the SBT/LZO/Si structure for use as a 1-T type FeRAM.

2 Experimental work

We prepared a $LaZrO_x$ (i.e., molar ratio of La/Zr=1) solution with 0.1 M concentration and the $Sr_{0.9}Bi_{2.1}Ta_2O_9$ solution with 0.3 M concentration, respectively.

To fabricate the LZO/Si structure, a p-type Si (100) wafer was used as a substrate. The substrate was dipped in a diluted HF solution to remove the native oxide from the surface of the Si. Then, we spin-coated the LZO solution on the cleaned Si wafer at 4000 rpm for 25 s. The coated LZO thin films were baked at 400°C for 10 min. Subsequently, the films, were annealed at 700, 750, and 800°C for 30 min in an O_2 atmosphere by rapid thermal annealing (RTA), respectively.

The SBT solution was also spin-coated on the LZO/Si structure at 3000 rpm for 20 s. The coated SBT film was dried at 250°C for 10 min on a hot-plate to remove the solvent. These processes were repeated to obtain the desired film thickness. Finally, the film was crystallized at 800°C for 30 min in an O_2 atmosphere by RTA. For electrical measurements of LZO/Si and SBT/LZO/Si structures, Au electrodes were thermally evaporated onto the surface of the samples. As a top electrode, we used a shadow mask patterned with 500 μm-diameter circles.

The surface morphology and crystallization quality of the LZO thin film and the SBT film were observed by using atomic force microscopy (AFM) and X-ray diffraction (XRD) measurements, respectively. The electrical characteristics of the Au/LZO/Si and the Au/SBT/LZO/Si structure were measured using a HP 4280A capacitance-meter and HP 4155C precision semiconductor parameter analyzer, respectively.

3 Results and discussion

Figure 1 shows the XRD patterns of the LZO films with different annealing temperatures. From the measurements, the peak, (331) and (511), of the fluorite type structure prevailed in the XRD patterns of the 700-°C-annealed LZO film and the peak, (222) and (400), of the pyrochlore type structure prevailed in the XRD patterns of 800-°C-annealed LZO film. In the case of the 750-°C-annealed LZO film, the weak peaks as (222), (331), and (511), were observed [17]. These facts meant that the phase of the LZO films was not an amorphous but rather a polycrystalline phase. In general, the crystallization temperature of the LZO film is around 1000–1200°C. However, the insulating buffer layer is desirable to keep the amorphous phase because grain boundaries of this layer provide the leakage paths. In addition, the surface roughness of the insulating buffer layer is a very important factor since it may have affected the leakage characteristics [18]. Figure 2 shows the surface morphological images of the LZO thin films measured by AFM. The measured area was 500×500 nm^2. The root-mean-squared (RMS) surface roughness of the LZO films were about 1.186, 0.365, and 0.469 nm for 700, 750, and 800°C, respectively. Interestingly, the surface roughness of the 750-°C-annealed LZO film was a little better than others. Therefore, the LZO films had very flat and smooth surface morphologies even though the crystalline phase was not amorphous.

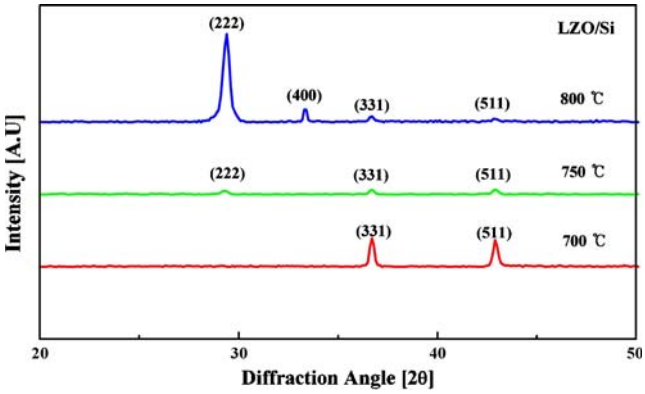

Fig. 1 The XRD patterns of LZO films with different annealing temperatures

Figure 3 shows the *C–V* characteristics of the LZO film with different annealing temperatures and the *J–V* characteristics of the 750-°C-annealed LZO thin film. The measurement of the *C–V* characteristics was performed with a ±5 V bias sweep at 1 MHz. As shown in this figure, no hysteresis was observed in the *C–V* curves for 700 and 750°C. We observed a little hysteresis in the *C–V* curve for 800°C. A little sloping tendency was shown in the accumulation region of the 700-°C-annealed sample. In particular, no hysteresis meant that there was little chance for a rechargeable oxide trap to exist at the interface between the LZO film and the Si substrate. On the other hand, the flat band was shifted in the negative direction as the annealing temperature increased. The equivalent oxide thickness (EOT) determined from the accumulation capacitance of the *C–V* curve was about 18 and 17.6 nm for 750

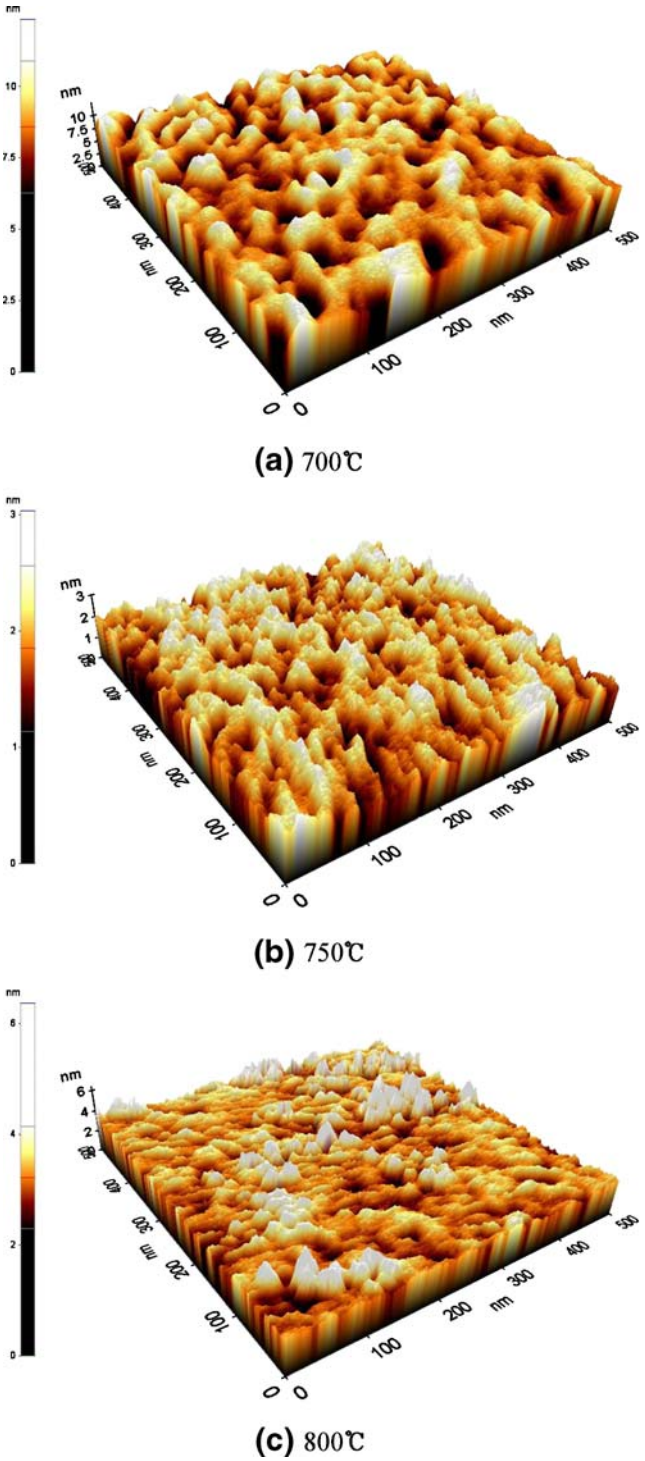

Fig. 2 Surface morphological images of (**a**) 700-°C-, (**b**) 750-°C-, and (**c**) 800-°C-annealed LZO film on Si

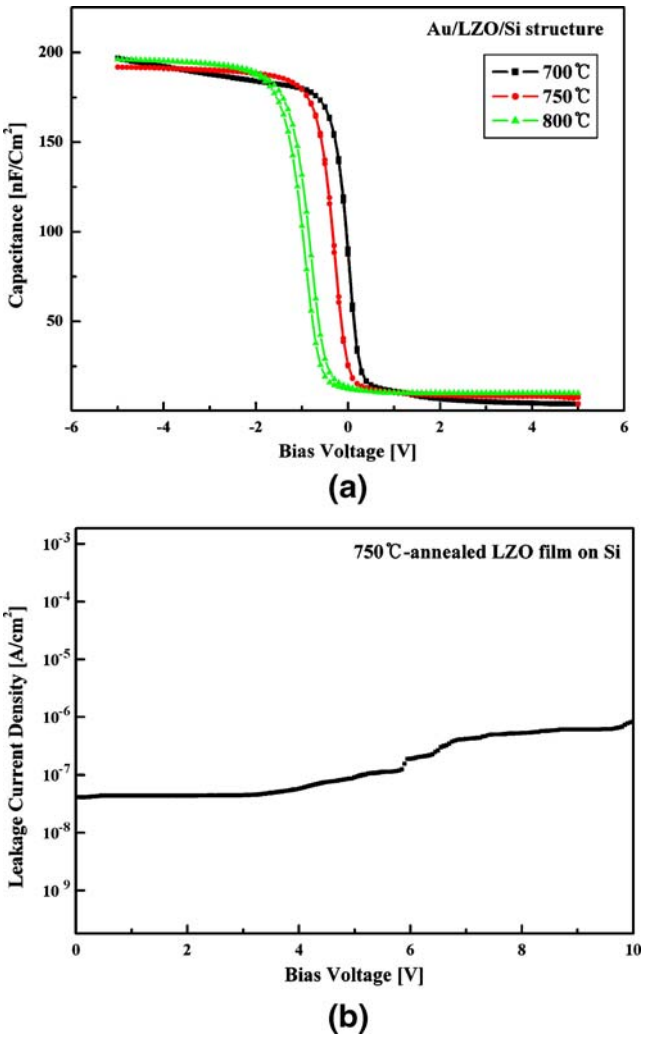

Fig. 3 (**a**) The *C–V* characteristics of the LZO film with different annealing temperatures and (**b**) the *J–V* characteristics of the 750-°C-annealed LZO on Si

and 800°C, respectively. The relatively large EOT was probably due to the formation of a degradation factor such as a low-*k* oxide region originated at the interface between the LZO film and Si substrate during the annealing process. In view of the results so far achieved, we decided to anneal the LZO film at 750°C. The leakage current density of the 750-°C-annealed LZO film was about 8.2×10^{-7} A/cm^2 at 10 V.

Figure 4 shows the *C–V* characteristics of the Au/SBT/LZO/Si structure with 150-nm-, 300-nm-, 450-nm-, and 600-nm-thick SBT films, which were measured at 1 MHz. For comparison, the capacitance values of each sample were normalized. As shown in the figure, hysteresis loops with a clockwise direction were observed, irrespective of the SBT film thickness. These were related to the ferroelectric behavior of the SBT film. The memory window width increased as the film thickness increased; whereas, the accumulation capacitance decreased.

Figure 5 shows the XRD pattern and the surface AFM image of the 600-nm-thick SBT film on the LZO/Si structure. According to the XRD pattern, the film was crystallized in a polycrystalline phase with a highly preferred (115) orientation. In general, film orientation is one of the important factors for ferroelectric properties,

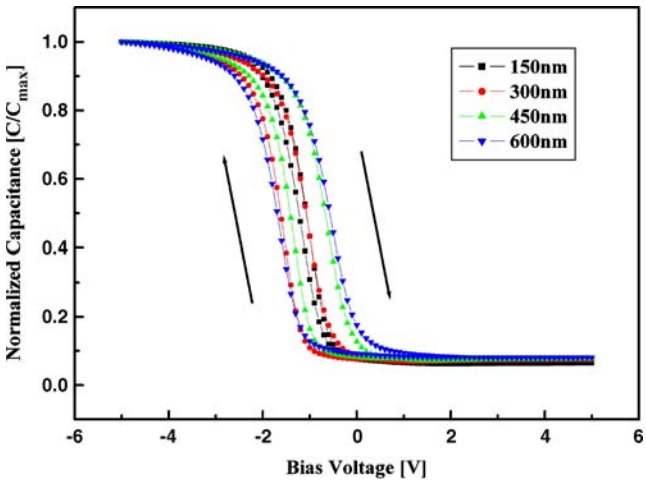

Fig. 4 *C–V* characteristics of the Au/SBT/LZO/Si structure with 150-nm-, 300-nm-, 450-nm-, and 600-nm-thick SBT films

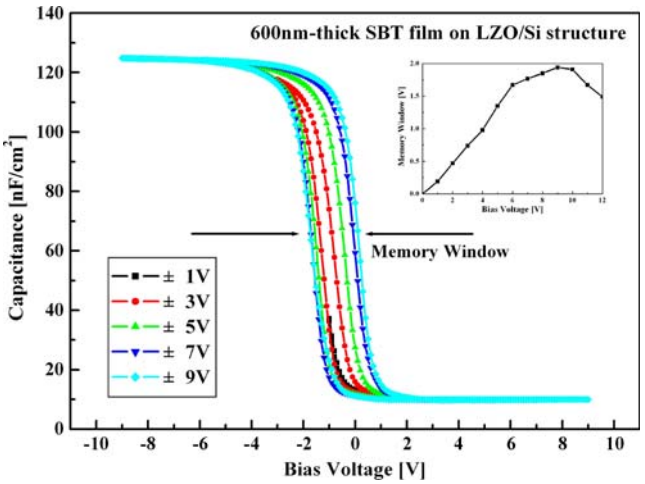

Fig. 6 Variations of the memory window width for the 600-nm-thick SBT film as a function of the bias sweep voltage

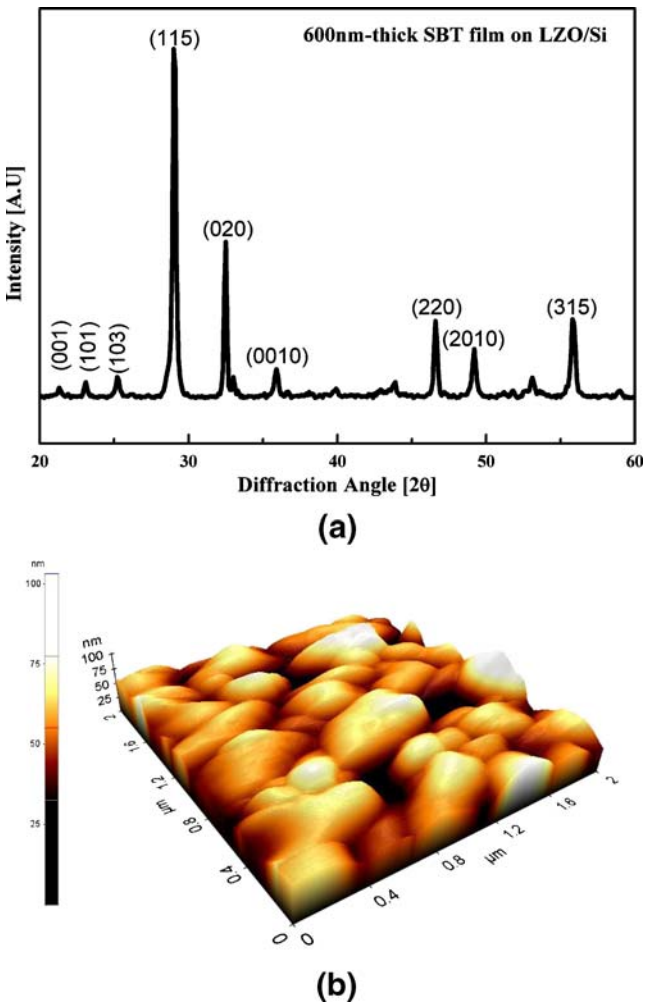

Fig. 5 (**a**) A typical X-ray diffraction pattern and (**b**) a surface morphological image of the 600-nm-thick SBT film

such as polarization, because it is related to the direction of the dipoles [19]. The magnitude of remanent polarization, affecting the characteristics of the film, depends on the orientation of ferroelectric film. From the surface AFM image of the 600-nm-thick SBT film, the average and RMS surface roughness were about 11.459 and 8.645 nm, respectively.

Figure 6 shows the memory window width of the Au/SBT/LZO/Si structure with 600-nm-thick SBT film for a variety of bias sweep voltages. The memory window width increased as the bias sweep voltage increased. However, when the applied sweep voltage exceeded ±9 V, the memory window width began to decrease. Maybe this decrease was a result of the charge injection. The maximum value of the memory window width was about 1.94 V at a bias sweep voltage of ±9 V.

Figure 7 shows *J–V* characteristics of the Au/SBT/LZO/Si MFIS structure with the 600-nm-thick SBT film at a bias

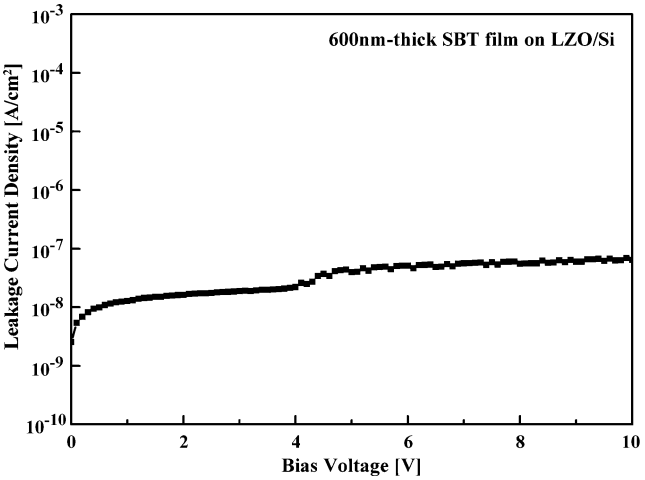

Fig. 7 *J–V* characteristics of the 600-nm-thick SBT film on a LZO/Si structure

voltage in the range of 0–10 V. The leakage current density was about 6.48×10^{-8} A/cm^2 at 10 V. The measured value of the leakage current density, one of the most important properties for a MFIS structure, showed relatively good characteristics. From the above several facts, we were able to determine that the LZO film was suitable in acting as an insulating buffer layer in a MFIS structure.

4 Conclusions

In this work, we fabricated a MFIS structure of Au/SBT/LZO/Si using the SBT film as a ferroelectric layer and the LZO film as an insulating buffer layer. The sol–gel deposited LZO film on the Si substrate had a good surface morphology even though its crystalline phase was not an amorphous one. We compared the *C–V* characteristics of the LZO films with different annealing temperatures and decided to anneal the LZO film at 750°C. The RMS surface roughness and EOT of the 750-°C-annealed LZO film were about 0.365 and 18 nm, respectively. Also, its leakage current density was about 8.2×10^{-7} A/cm^2 at 10 V. In the Au/SBT/LZO/Si structures, the memory window width increased with the increase of the bias sweep voltage and the SBT film thickness. The 600-nm-thick SBT film on the LZO/Si structure was crystallized in a polycrystalline phase with a highly preferred (115) orientation and showed a memory window width of about 1.94 V at a bias sweep voltage of ±9 V. Its leakage current density was about 6.48×10^{-8} A/cm^2 at 10 V.

From these results, we confirmed that the LZO film in the Au/SBT/LZO/Si structure effectively accomplished the role of the insulating buffer layer. However, the relatively large EOT of the LZO film should be improved for the ferroelectric random access memory application.

References

1. J.F. Scott, C.A. Paz de Araujo, Science **246**, 14004 (1989)
2. K. Takahashi, K. Aizawa, H. Ishiwara, Jpn. J. Appl. Phys **45**, 5098 (2006)
3. Y. Shichi, S. Tanimoto, T. Goto, K. Kuroiwa, Y. Tarui, Jpn. J. Appl. Phys **33**, 5172 (1994)
4. B.-E. Park, K. Takahashi, H. Ishiwara, J. Kor. Phys. Soc **46**, 346 (2005)
5. Y.-U. Song, J.-S. Park, J.-W. Yoon, G.-G. Lee, B.-E. Park, C.-J. Kim, Y.-S. Choi, J.-H. Koh, Int. Ferroeletr **84**, 203 (2006)
6. B.-E. Park, K. Takahashi, H. Ishiwara, Appl. Phys. Lett **85**, 4448 (2004)
7. B.-E. Park, H. Ishiwara, J. Kor. Phys. Soc **42**, S1149 (2003)
8. M. Takahashi, S. Sakai, Jpn. J. Appl. Phys **44**, L800 (2005)
9. H. Okuyucu, E. Celik, M.K. Ramazanoglu, T. Akin, I.H. Mutlu, W. Sigmund, J.E. Crow, Y.S. Hascicek, IEEE Trans. Appl. Supercond **11**, 2889 (2001)
10. J.W. Seo, J. Fompeyrine, A. Guiller, G. Norga, C. Marchiori, H. Siegwart, J.-P. Locquet, Appl. Phys. Lett **83**, 5211 (2003)
11. S. Tirumala, A.C. Rastogi, S.B. Desu, J. Electroceram. **5**, 7 (2000)
12. W.L. Chang, J.L. He, J. Electrocerm. **13**, 35 (2005)
13. W. Jo, Appl. Phys. A: Mater. Sci. Process **72**, 81 (2004)
14. A.Z. Simões, A.H.M. Gonzalez, C.S. Riccardi, E.C. Souza, F. Moura, M.A. Zaghete, E. Longo, J.A. Verela, J. Electroceram. **13**, 65 (2004)
15. E.F. Dudnik, V.M. Duda, A.I. Kushnerov, Phys. Solid State **43**, 2280 (2001)
16. H.S. Choi, E.H. Kim, I.H. Choi, Y.T. Kim, J.H. Choi, J.Y. Lee, Thin Solid Films **388**, 226 (2001)
17. H. Kido, S. Komarneni, R. Roy, J. Am. Ceram. Soc **74**, 422 (1991)
18. H. Hu, C. Zhu, Y.F. Lu, Y.H. Wu, T. Liew, M.F. Li, B.J. Cho, W. K. Choi, N. Yakovlev, J. Appl. Phys. **94**, 551 (2003)
19. M. Nagata, D.P. Vijay, X. Zhang, S.B. Desu, Phys. Stat. Sol **157**, 75(1996)